MITSUBISHI POWER

LSIOS01 I/O scanner card

Gigabit Ether 1000BASE-T specification compliant

■Summary

＊Main function	:	GbE-LVDS communication bridge
＊Operating ambient temperature range	:	-5 to 60℃
＊User interfaces		
・ Ethernet (1000BASE-T)	:	2 in total
・ Micro SD slots	:	1 in total
・ USB mini-B connector	:	1 in total
・ Switches	:	2 in total
- Reset switch		
- Abort switch		

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■Specification

ITEM		SPECIFICATION
Function		LVDS input-output communication Giga-bit Ethernet ring communication
Communication rate (LVDS)		100 Mbps
Number of addressing nodes		Max 96 nodes
EEPROM		2 kbit (For initial setting information of MAC address)
Ethernet interface		1000BASE-T : 2
Serial interface		USB Serial (USB miniB connector) : 1
User interface		Micro SD card : 1 Abort switch : 1 Reset switch : 1
Controller		Xilinx Spartan6
Self diagnosis		Clock abnormal check CRC check (FPGA) Memory check Power voltage check Configuration check
Data check method		CRC32
Indications		4: Power / Status / Mode / Access
Hot-swapping		Supported (*Note that emergency stop signal processing must be handled by user circuity)
Rated voltage		DC 24 V ±20% (Supplied from backplane)
Environmental conditions	Module ambient temperature	(Operating) -5 to 60℃
		(Storage) -40 to 85℃
	Module ambient humidity	(Operating / Storage) Less than 95% RH (No condensation)
Vibration		3.5 mm at 5 to 8.4 Hz, 1 G at 8.4 to 150 Hz
Shock		15 G 11 ms
Current consumption		272 mA
Weight		240 g or less
Size		112 mm (D) x 177.8 mm (H) x 25.8 mm (W) (Except projection)
Standard/Directive		IEC61131-2:2007, RoHS

*About compliant module type

For compliant modules of this product, please refer to " Compliant backplane list (CGS-S9901-E-XX) ".

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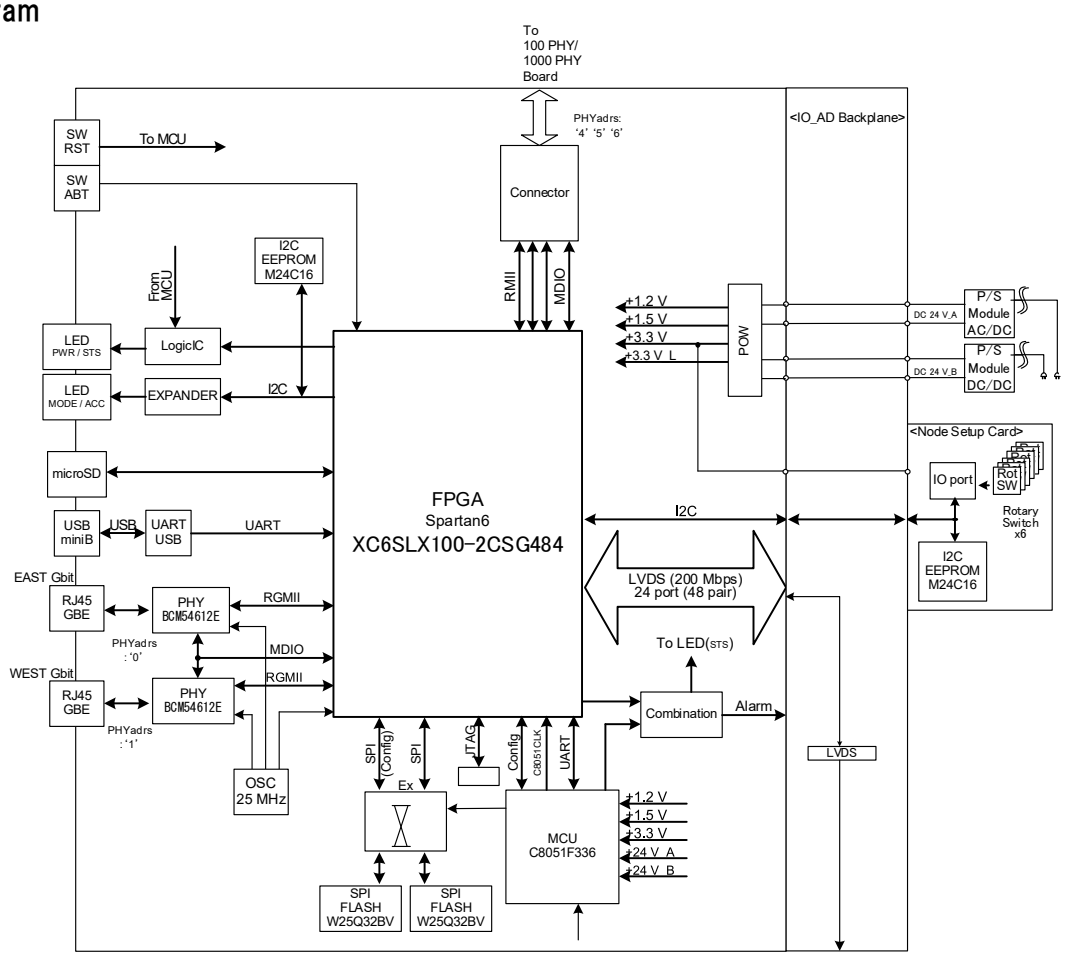
■Block diagram



P/S	;	Power Supply
IO_AD	;	Input/Output_Adapter
LVDS	;	Low Voltage Differential Signaling
FPGA	;	Field Programmable Gate Array
MCU	;	Micro controller Unit
Flash	;	Flash memory
CLK	;	Clock Oscillator
OSC	;	Oscillator
RST	;	Reset
LED	;	Light Emitting Diode
ABO	;	Abort
POW	;	Power
STS	;	Status
GBE	;	Giga bit Ether
UART	;	Universal Asynchronous Receiver Transmitter
EEPROM	;	Electrically Erasable Programmable Read-Only Memory
SPI	;	Serial Peripheral Interface
DDR3	;	Double Data Rate3
I2C	;	Inter-Integrated Circuit
JTAG	;	Joint Test Action Group
SW	;	Switch
PHY	;	Physical layer

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