

# LSIOA01-2 IO adapter module

Gigabit Ethernet 1000BASE-T Specification compliance

## ■ Summary



\* Major function : Giga-bit Ethernet-LVDS communication bridge

\* Module ambient temperature : -5 to 60°C

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## ■ Specifications

| ITEM                             |                            | SPECIFICATION  |
|----------------------------------|----------------------------|--|
| Function                         |                            | I/O module communication (LVDS)<br>Giga-bit Ethernet ring communication                                |
| Communication rate (LVDS)        |                            | 100 Mbps   |
| Number of D-Ring addressing node |                            | Maximum 96 node  |
| EEPROM                           |                            | 2 kbit (For initial setting information of MAC address)  |
| Ethernet interface               | For D-Ring                 | 1000BASE-T : 2   |
| User interface                   |                            | Abort switch : 1<br>Reset switch : 1<br>USB mini-B : 1   |
| Controller                       |                            | Xilinx Spartan7  |
| Self-diagnostic functions        |                            | Clock abnormal check<br>CRC check (FPGA)<br>Memory check<br>Power voltage check<br>Configuration check |
| Data check method                |                            | CRC32  |
| Indicator                        |                            | 4: PWR (Power)/STS (Status)/MOD (Mode)/ACC (Access)  |
| Hot swap                         |                            | Possible   |
| Power supply                     |                            | DC 24 V $\pm$ 20%/typ 0.24A (The voltage supplied from the backplane)                                  |
| Environmental conditions         | Module ambient temperature | (Operating) -5 to 60°C<br>(Storage) -40 to 85°C  |
|                                  | Module ambient humidity    | (Operating / Storage) 10 to 95% RH or less (No condensation)   |
| Vibration                        |                            | 3.5 mm @5 to 8.4 Hz<br>1 G @8.4 to 150 Hz  |
| Shock                            |                            | 15 G 11 ms 0.5 J $\pm$ 0.04 J  |
| Current consumption              |                            | Less than 262 mA   |
| Weight                           |                            | 0.22 kg  |
| Dimensions                       |                            | 112 mm (D) x 117 mm (H) x 46 mm (W) (Except projection)  |
| Standard/Directive               |                            | EN 61131-2:2007, RoHS  |

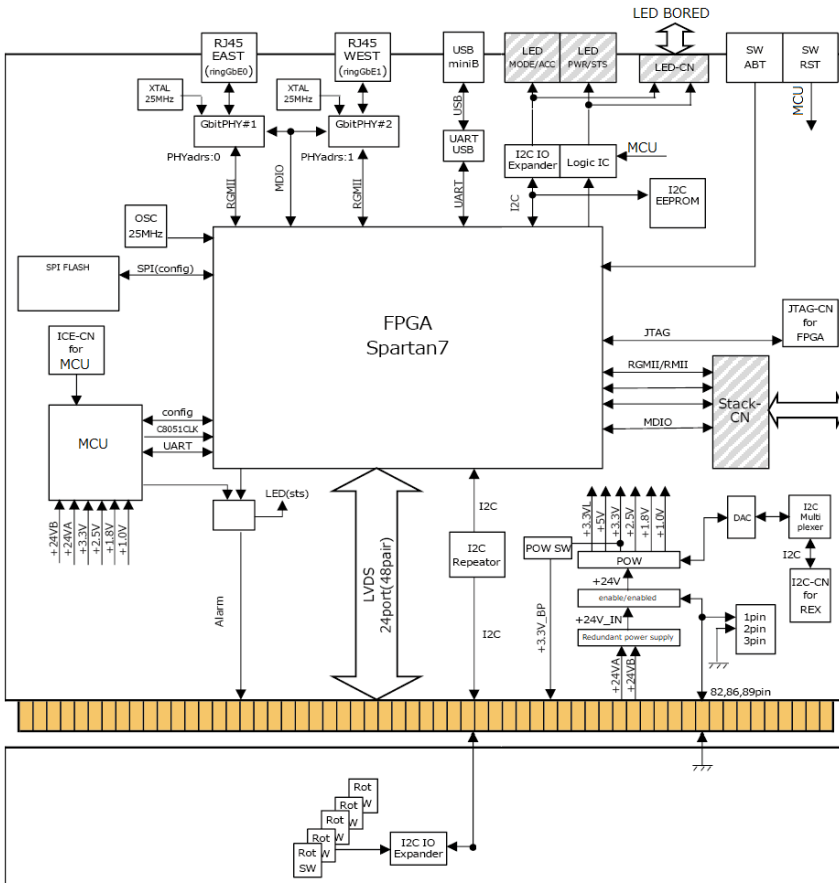
About compliant module type

For compliant modules of this product, please refer to "Compliant backplane list (CGS-S9901-E-XX)".

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## Block diagram



- P/S : Power Supply
- IO\_AD : Input/Output Adapter
- LVDS : Low Voltage Differential Signaling
- FPGA : Field Programmable Gate Array
- MCU : Micro controller Unit
- Flash : Flash memory
- CLK : Clock Oscillator
- OSC : Oscillator
- RST : Reset
- LED : Light Emitting Diode
- ABO : Abort
- PWR : Power
- STS : Status
- GBE : Giga bit Ether
- UART : Universal Asynchronous Receiver Transmitter
- EEPROM : Electrically Erasable Programmable Read-Only Memory
- SPI : Serial Peripheral Interface
- DDR3 : Double Data Rate3
- I2C : Inter-Integrated Circuit
- JTAG : Joint Test Action Group

When using, please read the instruction manual attached to the product carefully and use it properly.

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