

LSSCG01A Scanner Gateway module

Gigabit Ethernet 1000BASE-T Specification compliance Bridge unit for D-Ring (For optical communication expansion)

■ Summary



*Major function : Giga-bit Ethernet-LVDS communication bridge

*Module ambient temperature : -5 to 60°C

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■ Specifications

ITEM		SPECIFICATION
Function		I/O module communication (LVDS)
		D-Ring (Giga-bit Ethernet ring communication)
		Optical communication interface for expansion (100 Mbps multimode communication)
Number of D-Ring addressing node		Maximum 32 node
EEPROM		2 kbit (For initial setting information of MAC address)
Ethernet interface	For D-Ring	1000BASE-T : 2
Optical communication interface	For optical communication expansion	100BASE-FX : 3
		Connector type: LC Note) The connector shape of the LSSCG01 is MT-RJ, so when replacing LSSCG01 with LSSCG01A, prepare an adapter to convert the MT-RJ to LC, or replace the cable between the LSSCG01A and the optical termination box with an LC-SC cable. Cable specification: multimode50/125 μm or 62.5/125 μm
User interface		Abort switch : 1 Reset switch : 1 USB mini-B : 1
Controller		Xilinx Spartan7
I/O Communication	Communication method	LVDS
	Communication speed	100 Mbps
Self-diagnostic functions		Clock abnormal check CRC check (FPGA) Memory check Power voltage check Configuration check
Data check method		CRC32
Indicator		4: PWR (Power)/STS (Status)/MOD (Mode)/ACC (Access)
Hot swap		Possible
Power supply		DC 24 V ±20% (The voltage supplied from the backplane)
Environmental conditions	Module ambient temperature	(Operating) -5 to 60°C (Storage) -40 to 85°C
	Module ambient humidity	(Operating / Storage) 10 to 95% RH or less (No condensation)
Vibration		3.5 mm @5 to 8.4 Hz 1 G @8.4 to 150 Hz
Shock		15 G 11 ms
Current consumption		Less than 346 mA
Weight		0.35 kg
Dimensions		112 mm (D) x 117 mm (H) x 46 mm (W) (Except projection)
Standard/Directive		EN 61131-2:2007, RoHS

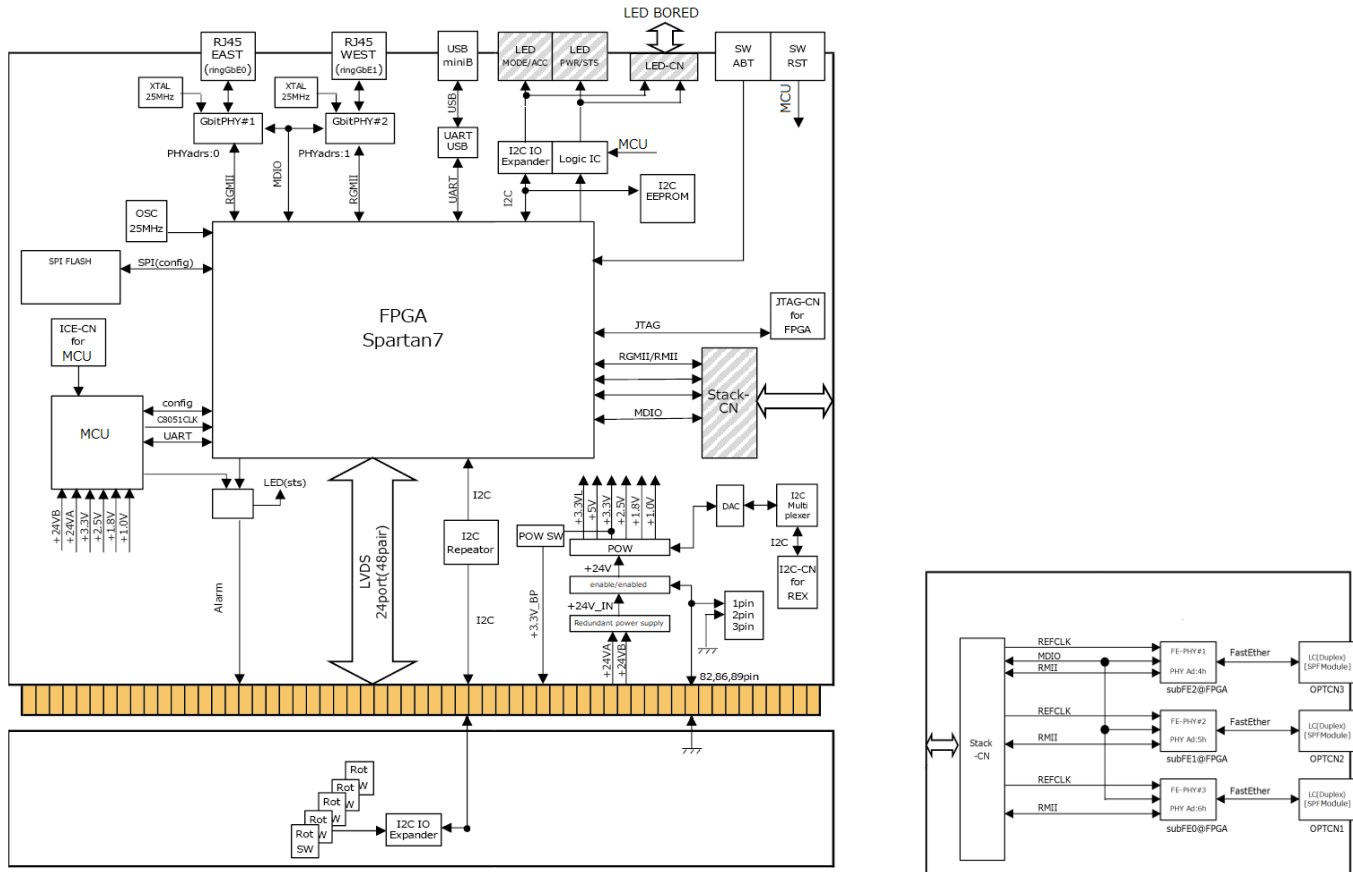
About compliant module type

For compliant modules of this product, please refer to "Compliant backplane list (CGS-S9901-E-XX)".

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Block diagram



- | | | |
|----------|---|---|
| P/S | : | Power Supply |
| I2C | : | Inter-Integrated Circuit |
| OPT-CN | : | Optical connector |
| RJ45_GBE | : | RJ45 connector _ Giga bit Ethernet |
| RMII | : | Reduced Media Independent Interface |
| MDIO | : | Management Data Input/Output Bus |
| FPGA | : | Field Programmable Gate Array |
| MCU | : | Micro controller Unit |
| UART | : | Universal Asynchronous Receiver Transmitter |
| JTAG | : | Joint Test Action Group |
| SPI | : | Serial Peripheral Interface |
| Flash | : | Flash memory |
| Ex | : | Exchange device |
| CLK | : | Clock Oscillator |
| OSC | : | Oscillator |
| EEPROM | : | Electrically Erasable Programmable Read-Only Memory |
| SW_RST | : | Reset switch |
| SW_ABO | : | Abort switch |
| LED | : | Light Emitting Diode |
| PWR/STS | : | Power/Status |
| MOD/ACC | : | Mode/Access |

When using, please read the instruction manual attached to the product carefully and use it properly.

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